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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/631,427	08/03/2000	Steven P. Larky	0325.00368	1792

21363 7590 11/05/2004

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EXAMINER	
DAY, HERNG DER	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/631,427	LARKY ET AL.	
	Examiner	Art Unit	
	Herng-der Day	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 21-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 21-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to Applicants' Amendment ("Amendment") to Office Action dated March 30, 2004, mailed June 30, 2004, and received by PTO July 2, 2004.

1-1. Claims 1-11 have been amended. Claims 12-20 have been cancelled. Claims 21-29 have been added. Claims 1-11 and 21-29 are pending.

1-2. Claims 1-11 and 21-29 have been examined and rejected.

Drawings

2. These replacement sheets of drawings are acceptable. The objection to the drawings has been withdrawn.

Specification

3. The objection to the specification has been withdrawn.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-11, 21-22, and 25-26 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable

one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

5-1. Claim 1 recites the limitation "generating one or more source signals by adding a digital signature to each of said analog signals" in step (B) of the claim. However, how to add a digital signature to an analog signal has not been disclosed in the specification. Therefore, without undue experimentation, it is unclear for one skilled in the art how to generate source signals by adding a digital signature to each of said analog signals.

5-2. Claim 9 recites the limitation "generating one or more attributed signals" in step (A) of the claim. As described at page 6 of the specification "The attributed analog signals (e.g., the analog signals each with an added digital signature)". However, how to add a digital signature to an analog signal has not been disclosed in the specification. Therefore, without undue experimentation, it is unclear for one skilled in the art how to generate attributed signals.

5-3. Claim 25 recites the limitation "(ii) add said digital signature to said analog signal" in lines 3-4 of the claim. However, how to add a digital signature to an analog signal has not been disclosed in the specification. Therefore, without undue experimentation, it is unclear for one skilled in the art how to add said digital signature to said analog signal.

5-4. Claims not specifically rejected above are rejected as being dependent on a rejected claim.

Claim Interpretation

6. Independent claim 1 recites the limitation "adding a digital signature to each of said analog signals". Independent claim 9 recites the limitation "generating one or more attributed

signals". Claim 25 recite the limitation "add said digital signature to said analog signal". All of them are rejected under 35 U.S.C. 112, first paragraph, because how to add a digital signature to an analog signal has not been disclosed in the specification as discussed in sections **5** to **5-4** above. For the purpose of claim examination with the broadest reasonable interpretation, the Examiner will interpret "adding a digital signature to an analog signal" as "generating a digital signature proportional to average supply current" which has been disclosed by Tabatabaei et al.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-11 and 21-29 are rejected under 35 U.S.C. 102(b) as being anticipated by tabatabaei et al., "A Current Integrator for BIST of Mixed-Signal ICs", 1999 17th IEEE VLSI Test Symposium, April 1999.

8-1. Regarding claim 1, tabatabaei et al. disclose a method for verification, comprising the steps of:

(A) generating one or more analog signals utilized by an analog design (I_{DD}, Figure 1);

(B) generating one or more source signals by adding a digital signature to each of said analog signals (n-bit N, Figure 1); and

(C) modeling said analog design using said source signals in place of said analog signals for verifying connectivity (discard this circuit, section 3, paragraph 1).

8-2. Regarding claim 2, tabatabaei et al. further disclose step (C) comprises the step of:

performing one or more simulations of said analog design with said source signals propagating through said analog design (simulation, section 3, paragraph 1).

8-3. Regarding claim 3, tabatabaei et al. further disclose each of said digital signatures corresponds to a type of said analog signals having a predetermined parameter (average supply current, abstract).

8-4. Regarding claim 44, tabatabaei et al. further disclose each of said digital signatures comprises a unique pulse width (n-bit N, Figure 1).

8-5. Regarding claim 5, tabatabaei et al. further disclose comprising the step of:

performing verification of said analog design (discard this circuit, section 3, paragraph 1).

8-6. Regarding claim 6, tabatabaei et al. further disclose performing said simulations further comprises the sub-step of:

verifying a connectivity of said analog signals through said analog design (discard this circuit, section 3, paragraph 1).

8-7. Regarding claim 7, tabatabaei et al. further disclose performing said simulations further comprises the sub-step of:

verifying a model of an analog block within said analog design configured to receive at least a particular one of said analog signals (for example, SIN2 were used as calibration signal, section 3, paragraph 1).

8-8. Regarding claim 8, tabatabaei et al. further disclose verifying said model further comprises the sub-step of:

verifying an output signal of said analog block for said digital signature associated with said particular one of said analog signals (for example, SIN2 were used as calibration signal, section 3, paragraph 1).

8-9. Regarding claim 9, tabatabaei et al. disclose method for testing a model of an analog device, comprising the steps of:

(A) generating one or more attributed signals each (i) having a unique digital signature and (ii) presented by a source block within said model of said analog device (n-bit N, Figure 1); and

(B) verifying connectivity of said attributed signals to a destination block within said model of said analog device by verifying reception of said unique digital signatures associated with each of said attributed signals at said destination block (discard this circuit, section 3, paragraph 1).

8-10. Regarding claim 10, tabatabaei et al. further disclose comprising the step of:

disabling processing of a particular one of said attributed signals if said particular signal is not verified at said destination block (discard this circuit, section 3, paragraph 1).

8-11. Regarding claim 11, tabatabaei et al. further disclose comprising the step of:

verifying a model of said destination block configured to receive at least one of said attributed signals (for example, SIN2 were used as calibration signal, section 3, paragraph 1).

8-12. Regarding claim 21, tabatabaei et al. further disclose each of said digital signatures comprises a plurality of pulses (n-bit N, Figure 1).

8-13. Regarding claim 22, tabatabaei et al. further disclose each of said digital signatures comprises a varying frequency signal (different frequency, section 3, paragraph 1).

8-14. Regarding claim 23, tabatabaei et al. disclose a system comprising:

a source for a plurality of signals, at least one of said signals representing an analog signal having a digital signature (I_{DD} and n-bit N, Figure 1).; and

a simulator connected to said source and configured to (i) simulate an analog design, (ii) receive said signals and (iii) verify a connectivity of said analog signal in said analog design using said digital signature (simulator, section 3, paragraph 1).

8-15. Regarding claim 24, tabatabaei et al. further disclose said source comprises an analog source block configured to generate said analog signal (I_{DD}, Figure 1).

8-16. Regarding claim 25, tabatabaei et al. further disclose said source further comprises an adder block configured to (i) generate said digital signature and (ii) add said digital signature to said analog signal (BICI, Figure 1).

8-17. Regarding claim 26, tabatabaei et al. further disclose said source further comprises a digital source block configured to generate at least one of said signals representing a digital signal (for example, FF1, Figure 6).

8-18. Regarding claim 27, tabatabaei et al. further disclose said digital signature comprises a plurality of pulses (n-bit N, Figure 1).

8-19. Regarding claim 28, tabatabaei et al. further disclose said pulses have a unique width to identify said analog signal (n-bit N, Figure 1).

8-20. Regarding claim 29, tabatabaei et al. further disclose said digital signature has a varying frequency (different frequency, section 3, paragraph 1).

Applicants' Arguments

9. Applicants argue the following:

9-1. (1) "Tabatabaei-l does not appear to disclose or suggest a step for generating one or more source signals by adding a digital signature to each of one or more analog signals as presently claimed" (page 15, paragraph 2, Amendment).

9-2. (2) "Tabatabaei-l appears to be silent regarding use of the digital signatures in modeling a design" (page 15, paragraph 3, Amendment).

9-3. (3) "Tabatabaei-l does not appear to disclose or suggest a step for verifying connectivity of an attributed signals from a source block to a destination block within a model of an analog device by verifying reception of unique digital signatures associated with each of the attributed signals the presently claimed" (page 16, paragraph 2, Amendment).

Response to Arguments

10. Applicants' arguments have been fully considered.

10-1. Applicants' argument (1) is not persuasive. Because how to add a digital signature to an analog signal has not been disclosed in the specification, for the purpose of claim examination with the broadest reasonable interpretation, the Examiner interprets "adding a digital signature to an analog signal" as disclosed by Tabatabaei et al. Therefore, Tabatabaei-l does disclose a step for generating one or more source signals by adding a digital signature to each of one or more analog signals.

10-2. Applicants' argument (2) is not persuasive. Simulation has been disclosed in section 3.

10-3. Applicants' argument (3) is not persuasive. Tabatabaei et al. disclose in section 3, for example, current lower threshold, tolerance band, and a decision to discard a circuit, which are related to verifying connectivity of a circuit with mixed-signal.

Conclusion

11. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Jean Homere can be reached on (571) 272-3780. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Herng-der Day H.D.
November 1, 2004

JEAN R. HOMERE
PRIMARY EXAMINER